IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please AMEND claims 11 and 12 in accordance with the following:

1. (PREVIOUSLY PRESENTED) A semiconductor device, comprising:

wire bonding connection pads at peripheral regions, surrounding an inside region, of an electrode terminal formation surface of a semiconductor chip;

test pads to test the semiconductor chip, arranged in the inside region; and

a plurality of rewiring patterns, extending from respective peripheral regions to the inside region of said electrode terminal formation surface, individual ones of the plurality of rewiring patterns connecting respective, individual electrode terminals and corresponding connection pads and test pads.

2. (PREVIOUSLY PRESENTED) A semiconductor device as set forth in claim 1, wherein:

the test pads are arranged in an array on the inside region.

3. (PREVIOUSLY PRESENTED) A semiconductor device as set forth in claim 1, wherein the electrode terminals are exposed through openings of a protective insulation layer covering said electrode terminal formation surface, the rewiring patterns extend on said protective insulation layer and are connected to said electrode terminals via said openings, said rewiring patterns and said protective insulation layer are further covered by an insulation layer, and said connection pads and said test pads, connected to said rewiring patterns, are exposed through openings in said insulation layer.

4. (PREVIOUSLY PRESENTED) A semiconductor device comprised of one or a stack of a plurality of the semiconductor devices as set forth in claim 1 as an element semiconductor device or a stack of one or more element semiconductor devices and a semiconductor chip carried on a wiring board, further comprising:

connection pads of each said element semiconductor device and connection electrodes of said wiring board being connected by wire bonding, and

each said element semiconductor device and/or each said semiconductor chip being sealed by resin on said wiring board.

5. (CANCELLED)

6. (CANCELLED)

7. (CANCELLED)

8. (CANCELLED)

9. (PREVIOUSLY PRESENTED) A semiconductor device as set forth in claim 2, characterized in that said electrode terminals are exposed through openings in a protective insulation layer covering said electrode terminal formation surface, said rewiring patterns extend on said protective insulation layer and are connected to said electrode terminals via said openings, said rewiring patterns and said protective insulation layer are further covered by an insulation layer, and said connection pads and said test pads connected to said rewiring patterns are exposed through openings in said insulation layer.

10. (CANCELLED)

11. (CURRENTLY AMENDED) A semiconductor device or a stack of a plurality of the semiconductor devices as set forth in claim 42 as an element semiconductor device or a stack of one or more of semiconductor devices and a semiconductor chip carried on a wiring board, further comprising:

connection pads of each said element semiconductor device and connection electrodes of said wiring board being connected by wire bonding, and

each said element semiconductor device and/or each said semiconductor chip being sealed by resin on said wiring board.

12. (CURRENTLY AMENDED) A semiconductor device comprised of one or a stack of a plurality of the semiconductor devices as set forth in claim 43 as an element semiconductor device or a stack of one or more of semiconductor devices and a semiconductor chip carried on a wiring board, further comprising:

connection pads of each said element semiconductor device and connection electrodes of said wiring board being connected by wire bonding, and

each said element semiconductor device and/or each said semiconductor chip being sealed by resin on said wiring board.